REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 8-26 are pending in this application. Claims 8-20 are allowed. Claims 22 and 25 were rejected under 35 U.S.C. § 112, first paragraph. Claims 21-26 were rejected under 35 U.S.C. § 112, first paragraph. Claims 24 and 26 were rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. patent 6,144,093 to Davis et al. (herein "Davis") in view of U.S. patent 5,925,926 to Watanabe.

Initially, applicants and applicants' representative wish to thank Examiners Im and Lee for the interview granted applicants' representative on December 15, 2003. During that interview the outstanding rejections were discussed in detail. Further, during that interview applicants' representative presented claim amendments and comments as to how the claims were fully supported by the original specification and as to how the claims distinguished over the applied art. The Examiners indicated they would further consider such comments and amendments when formally considered in a filed response.

Addressing now the rejection of claims 22 and 25 under 35 U.S.C. § 112, first paragraph, that rejection is traversed by the present response.

The above-noted claims were rejected as the specification was deemed to not disclose the covering of the diode region by an inner lead frame. However, applicants respectfully traverse that position.

Specifically, applicants draw attention to Figures 7A – 7C and Figure 8 in the present specification.

Initially, with reference to Figures 7A and 7B, those figures show two semiconductor chips 9_1 and 9_2. As clearly shown in those figures those two semiconductor chips 9_1 and 9_2 are covered by lead frames 15_1 and 15_2. Figure 8 shows a package of two chips Q1 and Q2. The chip Q2 includes a Schottky barrier diode SBD. The specification also specifically states

"the application of Q2 and Q1 to the sixth embodiment [which is shown in Figures 7A and 7B] ***as the first and second semiconductor chips*** allows part of the synchronous rectifier to be formed into one package".[1]

From the above teachings it is clear that the specification clearly states that the chips 9_2 and 9_1 in Figures 7A and 7B can be the respective chips Q2 and Q1 in Figure 8. From such teachings it is clear to one of ordinary skill in the art that when the semiconductor chips 9_2 and 9_1 are Q2 and Q1 from Figure 8, the Schottky diode SBD is covered by an inner lead frame 15_2.

Thus, the specification is believed to clearly support the features recited in claims 22 and 25.

Addressing now the rejection of claims 21-26 under 35 U.S.C. § 112, first paragraph, that rejection is also traversed by the present response.

The above-noted rejection is similar to the rejection directed to claims 22 and 25 noted above and is believed to be traversed for similar reasons.

Also, applicants point out that the inclusion of claim 24 in the rejection appears improper as claim 24 does not in fact recite an inner lead frame covering a Schottky diode, as was the basis for the rejection to claim 24. To address the specific comments noted in the Office Action that "Figures 7A-7C of the Application show a formation of two MOSFETS, not a formation of a MOSFET and a *Schottky diode*. And Fig. 7A shows that the inner lead frame (5) covers only the portion of the source electrodes (15_1, 15_2)"[2], that position is also traversed. First, as noted above the specification makes it explicit that the semiconductor chips 9_2 and 9_1 in Figure 7A can correspond to the elements Q2 and Q1 of Figure 8,

[1] See specifically the present specification at page 18, lines 4-7. [Emphasis added].
[2] Office Action of October 9, 2003, page 3, lines 8-10

respectively. Thus, the specification fully supports the Schottky diode SBD being part of a chip covered by the inner lead frame 15_2.

Applicant's also point out that element 5 is not the inner lead frame, but instead the inner lead frame is, e.g., elements 15_1 and 15_2. Element 5 is an inner lead connecting pad that connects to the inner lead frame.

In view of the above, it is respectfully submitted that each of claims 21-26 is also in full compliance with all requirements under 35 U.S.C. § 112, first paragraph.

Addressing now the rejection of claims 24 and 26 under 35 U.S.C. § 103(a) as unpatentable over Davis in view of Watanabe, that rejection is traversed by the present response.

Applicants believe that the outstanding grounds for rejection is not fully considered that in claim 24 the Schottky diode is part of the claim transistor chip. Specifically, claim 24 specifically recites "a transistor chip having ... a transistor region including a transistor, ... and a diode region in which a Schottky diode is connected in parallel to the transistor". Thus, clearly the Schottky diode is part of the claimed "transistor chip".

With reference to Figure 8 in the present specification as an example, a transistor chip Q2 includes the Schottky diode SBD. Such features are believed to clearly distinguish over the applied art.

Watanabe discloses in Figure 3 a Schottky diode 32 formed as a discrete chip separately from the MOSFET 30. Clearly the MOSFET 30 and the Schottky diode 32 in Davis are not part of the same transistor chip.

Further, in Davis the package lead 28 is connected to the source electrode 38 by a bonding wire 44, and to the Schottky diode 32 by the bonding wire 42.

In contrast to such a structure in Davis, in claim 24 the inner lead frame is connected to the first main electrode of the transistor chip, and thereby as the Schottky diode and the

transistor are part of the transistor chip, the inner lead frame is connected to the transistor and the Schottky diode. Again such a feature is in contrast to the teachings in Davis.

Moreover, no teachings in Watanabe can overcome the deficiencies in Davis.

Although Watanabe discloses an inner lead, the inner lead is connected to an electrode on the chip and package lead (outer lead) in a one-to-one relationship. As a result the bonding wires 42 and 44 of Davis cannot be replaced with the inner lead of Watanabe.

Moreover, Watanabe simply does not overcome the above-noted deficiencies in Davis.

In such ways, claims 24 and 26 are believed to distinguish over the combination of teachings of Davis in view of Watanabe.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested this case be passed to issue.

Respectfully submitted,

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